REMARKS

Claims 1-18 were examined in the August 12, 2004 office action. In that action, the examiner objected to the specification on the basis that the abstract included reference and figure numbers. The foregoing amendment presents a substitute abstract lacking the matter that was objected to.

The examiner also objected to claims 8 and 16 on the basis that the claims on which they depend do not teach a decoder. That objection is not clearly understood since these claims present, as additional limitations, a channel decoder or a channel decoding step. The undersigned surmises that the examiner may have intended an objection based on failure to specify that the received signal has been channel coded, and so claims 8 and 16 have been amended to so specify.

The examiner also rejected claims 1-18 on prior art grounds. For the following reasons, it is respectfully submitted that claims 1-18 are patentable.

The present invention includes, *inter alia*, encoded signals having data and components that can be processed to detect errors, wherein a receiver lacking error detection circuitry can still process the encoded signal to extract the data. The invention enables new systems to incorporate error detection while maintaining backward compatibility with existing systems that lack error detection. Prior art systems like that disclosed in U.S. Patent No. 5,341,384 to Miya et al. ("Miya") lack such backward compatibility. Such systems calculate a checksum for an input signal, add it to the signal, and then encode the resulting signal for transmission to enable error correcting upon transmission; such encoded signals cannot be processed properly by equipment that lacks error detection and checksum monitoring. (Application at page 1, lines 6-22.)

The § 102 Rejections

The examiner rejected claims 1, 3-8, 17, and 18 under 35 U.S.C. § 102(e) as anticipated by

U.S. Patent No. 6,658,378 to Maeda. This rejection is respectfully traversed, for the following reasons.

The examiner rejected claim 1 based on Maeda's disclosure at col. 5, lines 15-40 and 45-52. In stating the rejection, the examiner did not identify elements of the claim and state where in Maeda those elements are found. Instead, the examiner merely restated what Maeda discloses at the cited locations, without any connection to the claim language. It is respectfully submitted that such a rejection is improper under 37 C.F.R. § 1.104(c)(2), in that the pertinence of the cited portions to the claim is not stated.

In any event, Maeda is no more pertinent to the claims than the Miya patent referenced above, which was discussed in the application as background art. Compare Maeda Fig. 25, elements S1, S2, and S3, with Miya Fig. 1, elements 2, 3, and 4. Maeda and Miya disclose encoding a set of input bits, calculating checksum bits for the encoded input bits, concatenating the encoded input bits and the checksum bits, and channel coding the concatenated bitstream for transmission. See Miya, col. 2 lines 37-47, and Maeda, col. 6 lines 9-21. Neither Maeda nor Miya discloses calculating a checksum on one or more packets of input data, then encoding the packet(s) of input data, and adding the checksum to the encoded packet(s) of input data to form an encoded signal, as claimed in claim 1 (in fact, Maeda does not refer to packets at all). Similarly, Maeda does not disclose the corresponding process of receiving and decoding such a signal, as claimed in claim 5.

The rejection of claim 4, which recites the further step of channel encoding, and claim 8, which recites the further step of channel decoding a channel-encoded signal, is highly illuminating. Certainly Maeda discloses channel (transmission path) encoding and decoding, in blocks 4 and 14, respectively. However, the processes in Maeda blocks 4 and 14 are the very ones that the examiner relied on to reject claims 1 and 5. Maeda does indeed show the "further" steps of channel encoding

and decoding; this clearly illustrates that Maeda does *not* show the previously set forth encoding and decoding of claims 1 and 5. The examiner cannot count the channel coding of Maeda as satisfying different limitations in applicant's independent and dependent claims.

The § 103 Rejections

The examiner rejected claim 2 under 35 U.S.C. § 103(a) as unpatentable over Maeda in view of U.S. Patent No. 5,343,527 to Knecht et al. ("Knecht") at col. 3 lines 28-45. Although Knecht does refer to checksum packets, Maeda does not refer to packets at all, and Knecht does not suggest a modification of Maeda to calculate a checksum of an input data packet, encode the input packet, and transmit the checksum as a packet along with the encoded input packet.

The examiner also rejected claims 9-16 under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 6,178,535 to Kajala et al. ("Kajala") in view of Knecht. Kajala, like Maeda and Miya, discloses encoding an input signal, calculating a CRC for the encoded signal, appending the CRC to the encoded signal, and encoding the resulting signal It does not disclose calculating a checksum for the input, encoding the input, and combining the encoded input with the checksum, as claimed.

The New Claims

New claims 19-20 add limitations regarding DST coding of DSD audio signals, and inserting the checksum packet in an audio information field. They are supported in the application, *inter alia*, at pages 4-5. It is believed that the additional limitations of these claims further patentably distinguish them.

Conclusion

Reconsideration and further examination is requested, and an early and favorable action is earnestly solicited.

Respectfully submitted,

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